**CMPEN 371: Advanced Digital Design**

**Fall 2016**

**Lab 7: PS/2 Keyboard Interface**

**Due: 26 October 2016**

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**ACKNOWLEDGEMENT**

This work is entirely our own and I did not provide any assistance except as noted. The approximate contribution of each team member is as follows:

{50%} Saw Xue Zheng  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

{50%} Krishna Ramesh \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Grading Rubric**

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| --- | --- |
| **Criteria** | **Grade** |
| Design (Sound algorithm, good block diagrams / state diagrams / state tables, efficient design, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Translate to VHDL (VHDL matches design docs, good comments / whitespace, follows guidelines, efficient coding, etc.)  Excellent: 6; Good: 4; Satisfactory: 2; Unsatisfactory: 0; Failure: -2 or worse | / 6 |
| Test in Simulator (test bench or script for each component and FSM, good coverage, components / FSMs verified, etc.)  Excellent: 3; Good: 2; Satisfactory: 1; Unsatisfactory: 0; Failure: -1 or worse | / 3 |
| Test in Hardware (demo in lab)   * Last four scan codes displayed * State of the arrow keys displayed on LEDs * (X,Y) coordinate displayed, arrow keys move it while pressed * Other | / 35 |
| Bonus (optional challenge, etc.) |  |
| Penalty (late demo, late submission on Canvas, team member absent from demo, etc.)  Demo late in lab: -2; Demo up to 5 days late: -5; Demo more than 5 days late: -10  Submitted late or incompletely on Canvas: -5; Not submitted on Canvas: no grade for lab |  |
| TOTAL | / 50 |

**DESIGN**

The following design documents are attached:

Filename Description

L07-01.pdf Top level block diagram

L07-02.pdf Block diagram for ScanCodeReader

L07-03.pdf FSM for ScanCodeReader

L07-04.pdf Block diagram for ScanCodeReader Datapath

L07-05.pdf Block diagram for PS2KBProcessor

L07-06.pdf FSM for PS2KBProcessor

L07-07.pdf

L07-08.pdf Block diagram for PS2KBProcessor

Datapath

**TRANSLATE TO VHDL**

The following HDL models are attached:

Filename Description

Lab07\_xps5001\_kmr5802.vhd Top Level: Top level vhd file

PS2KBD\_ScanCodeReader.vhd Component: ScanCodeReader for PS/2

ScanCodeReadFSM.vhd FSM for ScanCodeReader

ScanCodeReadDataPath.vhd Datapath for ScanCodeReader

ScanCodeProcessor.vhd Component: Processor for PS/2 Keyboard ScanCodes

PS2KBFSM.vhd FSM for ScanCodeProcessor

PS2KBDP.vhd Datapath for ScanCodeProcessor

The following HDL models and other files are not attached but are submitted electronically:

Filename Description

TimeOut.vhd Component: Timeout component

**TEST IN SIMULATOR**

None. Test were performed manually on hardware.

**TEST IN HARDWARE**

The program successfully was put on the board and works as expected.

**PERFORMANCE**

The following cost and performance metrics were obtained:

Area (resources used)

Number of Slice Registers: 187

Number of Slice LUTs: 220

Delay

Minimum Period: 6.132 ns

Maximum Frequency 163 MHz

The critical path goes from *20hz\_pulse\_generator*, through *xcord:updowncounter*, to *xcord:Q*

**QUESTIONS**

(There are no questions for this lab)